Amendments To The Specification

1. Please substitute the following amended paragraph for the original paragraph that begins on page 4, line 15.

As shown, the bus system 22 includes a "virtual" memory bus 30, a "physical" memory bus 32 and a single data bus 34. Each of these two memory buses include respective control lines 38, 42 and address lines 36, 40. As will be described in greater detail below, the virtual memory bus 30 is used as a communication path for virtual addresses. These virtual addresses may be transmitted from the CPU 12, the first DMA controller 26 or the second DMA controller 27 and are received by the ATU 24. The physical memory bus 32 is used as a communication path for physical addresses which are transmitted from the ATU 24.

2. Please substitute the following amended paragraph for the original paragraph that begins on page 5, line 10.

As shown in FIG. 2, at the beginning of a write operation (step 202), the virtual bus master places a virtual address and appropriate control signals over the virtual address bus 30 (step 204). Next, the virtual bus master places the data on the data bus 34 (step 206). The virtual bus master then waits until an acknowledgment signal is received (step 208). As will be discussed below, this signal is generated by the ATU 24. Next, the bus master determines if there is additional data to write (step 210). If so, then the steps 204-210 are repeated. This operation continues until the write operation is complete (step 204). A read operation is performed in a similar manner.